IN THE SPECIFICATION

Please amend the specification as follows:

The sub-title on page 1, line 7 is amended as follows: Related Application ~~Invention~~

The two paragraphs on page 1, lines 8-12 are amended as follows:

The present application ~~invention~~ is related to the following application ~~invention~~ which is assigned to the same assignee as the present application ~~invention~~ and which was filed on even date herewith:

Serial No. 09/631,037, entitled "Electronic Assembly Comprising Substrate with Embedded Capacitors ~~and Methods of Manufacture~~", now U.S. Pat. No. 6,611,419.

The sub-title on page 1, line 14 is amended as follows: Technical Field ~~of the Invention~~

The paragraph beginning on page 1, line 15 is amended as follows:

The ~~present~~ application ~~invention~~ relates generally to electronics packaging. More particularly, the ~~present~~ application ~~invention~~ relates to an electronic assembly that includes an interposer having one or more embedded capacitors to reduce switching noise in a high-speed integrated circuit, and to manufacturing methods related thereto.

The sub-title on page 1, line 20 is amended as follows: Background Information ~~of the Invention~~

The three paragraphs on page 3, lines 11-19 are amended as follows:

FIG. 1 is a block diagram of an electronic system incorporating at least one electronic assembly with embedded capacitors in accordance with an [[one]] embodiment of the invention;

FIG. 2 shows a cross-sectional representation of a multilayer interposer in accordance with an [[one]] embodiment of the invention;

FIG. 3 shows a cross-sectional representation of a multilayer interposer with embedded capacitors in which the vias that couple capacitive layers of like potential are arranged throughout the interior of the interposer in accordance with an [[one]] embodiment of the invention;

The two paragraphs on page 3, lines 26-30 are amended as follows:

FIG. 6 shows a graphical representation of capacitance versus area for various dielectric materials that can be used in an interposer with an embedded capacitor in accordance with an [[one]] embodiment of the invention;

FIG. 7 is a flow diagram of a method of fabricating an interposer comprising an embedded capacitor, in accordance with an [[one]] embodiment of the invention; and

The paragraph beginning on page 4, line 1 is amended as follows:

FIG. 8 is a flow diagram of a method of fabricating an electronic assembly having an interposer comprising an embedded capacitor, in accordance with an [[one]] embodiment of the invention.

The sub-title on page 4, line 5 is amended as follows: Detailed Description ~~of Embodiments of the Invention~~

The four paragraphs beginning on page 4, line 6, and ending on page 5, line 12, are amended as follows:

In the following detailed description of embodiments of the invention, reference is made to the accompanying drawings that ~~which~~ form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventive subject matter ~~inventions~~ may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the inventive subject matter ~~invention~~, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventive subject matter ~~inventions~~. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of embodiments of the ~~present~~ inventive subject matter ~~invention~~ is defined only by the appended claims.

The ~~present~~ inventive subject matter ~~invention~~ provides a solution to power delivery problems that are associated with prior art packaging of integrated circuits that operate at high clock speeds and high power levels by embedding one or more decoupling capacitors in a

multilayer structure. Various embodiments are illustrated and described herein. In an [[one]] embodiment, the multilayer structure takes the form of an "interposer" between an IC die and a substrate to which the die would ordinarily have been directly mounted. The embedded capacitors can be discrete capacitors, or they can be one or more layers of capacitive material.

FIG. 1 is a block diagram of an electronic system 1 incorporating at least one electronic assembly 4 with embedded capacitors in accordance with an [[one]] embodiment of the invention. Electronic system 1 is merely one example of an electronic system in which the inventive subject matter ~~present invention~~ can be used. In this example, electronic system 1 comprises a data processing system that includes a system bus 2 to couple the various components of the system. System bus 2 provides communications links among the various components of the electronics system 1 and can be implemented as a single bus, as a combination of busses, or in any other suitable manner.

Electronic assembly 4 is coupled to system bus 2. Electronic assembly 4 can include any circuit or combination of circuits. In an [[one]] embodiment, electronic assembly 4 includes a processor 6 which can be of any type. As used herein, "processor" means any type of computational circuit, such as but not limited to a microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set computing (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, a graphics processor, a digital signal processor (DSP), or any other type of processor or processing circuit.

The paragraph beginning on page 6, line 1 is amended as follows:

FIG. 2 shows a cross-sectional representation of a multilayer interposer 50 in accordance with an [[one]] embodiment of the invention. Interposer 50 is interposed between IC die 40 and primary substrate 60. IC die 40 can be of any type, such as a microprocessor or microcontroller, memory circuit, application specific integrated circuit (ASIC), digital signal processor (DSP), a radio frequency circuit, an amplifier, a power converter, a filter, a clocking circuit, and the like. Primary substrate 60 can be of any suitable type and can be made of any suitable material, e.g. an organic material, a polyimide, silicon, glass, quartz, ceramic, and the like.

The paragraph beginning on page 6, line 17 is amended as follows:

The Vcc and Vss electrodes of capacitor 55 of interposer 50, represented by reference numerals 52 and 54, respectively, can be coupled by metallized power vias 48 and 49, respectively, to the corresponding bumps 43 and 45, respectively, at the central or core region of the die and to corresponding bumps 63 and 65, respectively, on the primary substrate 60. If it is assumed, for the embodiment illustrated, that the via pitch is approximately 150 microns, a large number of such power vias (in excess of 2,000) can be accommodated, coupling capacitor 55 directly to the Vcc and Vss power nodes or bumps of IC die 40. This ensures a very low value for the loop inductance and enhances the current carrying capability of the overall IC packaging structure.

The paragraph beginning on page 7, line 14 is amended as follows:

The inventive subject matter ~~invention~~ is equally applicable to embodiments where signal traces occur other than at the periphery, and to embodiments where Vcc and Vss traces are provided anywhere on the die. Essentially, all signal I/O levels from signal I/O bumps on the IC die 40 can be coupled through interposer 50 to its opposite surface using through-vias like vias 46 and 51 shown in FIG. 2. Likewise, Vcc and Vss levels from corresponding bumps on the IC die 40 can be coupled through interposer 50 to its opposite surface using through-vias like 48 and 49, respectively.

The paragraph beginning on page 8, line 20 is amended as follows:

FIG. 3 shows a cross-sectional representation of a multilayer interposer 310 with embedded capacitors in which the vias that couple capacitive layers of like potential are arranged throughout the interior of the interposer in accordance with an [[one]] embodiment of the invention. Interposer 310 can be coupled between IC die 300 and primary substrate 320. Interposer 310 can be coupled to IC die 300 by suitable connectors such as solder balls 301 on a matrix having the same pitch and location as corresponding conductive leads on IC die 300. Solder balls 301 can be affixed to lands 302 and 305 of interposer 310. Lands 302 are intended to be coupled to a Vcc potential, while lands 305 are intended to be coupled to a Vss potential.

Lands 302 are coupled to capacitive plates 306, whereas lands 305 are coupled to capacitive plates 307.

The paragraph beginning on page 10, line 26 is amended as follows:

Embedded capacitor 430 can be of any suitable type. In an [[one]] embodiment, it is a ceramic chip capacitor that is fabricated using conventional ceramic chip capacitor technology. While a single capacitor 430 is illustrated, for the sake of simplicity of illustration and description, multiple capacitors could be used in the embodiment illustrated in FIG. 4.

The two paragraphs on page 12, lines 6-15 are amended as follows:

Embedded capacitors 530 and 540 can be of any suitable type. In an [[one]] embodiment, they are ceramic chip capacitors that are fabricated using conventional ceramic chip capacitor technology. While two capacitors 530 and 540 are illustrated, for the sake of simplicity of illustration and description, a different number of capacitors could be used in the embodiment illustrated in FIG. 5, including only one capacitor.

FIGS. 2-5 are merely representational and are not drawn to scale. Certain proportions thereof may be exaggerated, while others may be minimized. FIGS. 2-5 are intended to illustrate various implementations of the inventive subject matter ~~invention~~, which can be understood and appropriately carried out by those of ordinary skill in the art.

The paragraph beginning on page 12, line 22 is amended as follows:

Although it is known in ceramic technology to embed low Dk capacitors in ceramic substrates, by sandwiching thin (e.g. 2 mils) films of conventional ceramic such as Al_2O_3 between metal planes, in embodiments of the present invention multilayer stacks of high Dk ply are used in an [[one]] embodiment. High Dk ply is commercially available for fabricating ceramic chip capacitors, for example. Suitable high Dk materials, such as titanate particles, can be inserted into the conventional ceramic matrix. Multilayer stacks of high Dk ply, such as $BaTiO_3$, in embodiments of the present invention can provide capacitances as high as 10 μF/sq. cm., compared to capacitances in the range of only nano-Farads/sq. cm. for low Dk ply.

The paragraph beginning on page 14, line 1 is amended as follows:

FIG. 6 shows a graphical representation of capacitance (in nano-Farads) versus a side dimension of the capacitor (in microns) for various dielectric materials that can be used in an interposer with an embedded capacitor in accordance with an [[one]] embodiment of the invention. Shown in FIG. 6 are plots for the following dielectric materials: line 601 for PZT (Dk=2000), line 602 for $BaTiO_3$ (Dk= 1000), line 603 for BST (Dk=500), line 604 for $SrTiO_x$ (Dk=200), and line 605 for TaO_x (Dk=25).

The two paragraphs on page 14, lines 17-25 are amended as follows:

FIG. 7 is a flow diagram of a method of fabricating an interposer comprising an embedded capacitor, in accordance with an [[one]] embodiment of the invention. The method begins at 701.

In 703, at least one capacitor having first and second terminals is formed within a structure. In an [[one]] embodiment, the structure is a multilayer ceramic structure, although in other embodiments the structure could be formed of a material other than a ceramic material. The capacitor comprises (1) at least one high permittivity layer sandwiched between conductive layers; alternatively, the capacitor is (2) a discrete capacitor.

The paragraph beginning on page 15, line 14-16 is amended as follows:

FIG. 8 is a flow diagram of a method of fabricating an electronic assembly having an interposer comprising an embedded capacitor, in accordance with an [[one]] embodiment of the invention. The method begins at 801.

Delete the sub-title entitled "Conclusion" on page 16, line 8.

The five paragraphs beginning on page 16, line 9, and ending on page 17, line 11, are amended as follows:

Embodiments of the inventive subject matter provide ~~The present invention provides~~ for an electronic assembly and methods of manufacture thereof that minimize problems, such as switching noise, associated with high clock frequencies and high power delivery. Embodiments

of the inventive subject matter provide ~~The present invention provides~~ scalable high capacitance (e.g. >10 mF/square centimeter) by employing embedded decoupling capacitors having low inductance that ~~which~~ can satisfy the power delivery requirements of, for example, high performance processors. An electronic system that incorporates the inventive subject matter ~~present invention~~ can operate at higher clock frequencies and is therefore more commercially attractive.

As shown herein, the inventive subject matter ~~present invention~~ can be implemented in a number of different embodiments, including an interposer, an electronic assembly, an electronic system, a data processing system, a method for making an interposer, and a method of making an electronic assembly. Other embodiments will be readily apparent to those of ordinary skill in the art. The capacitive elements, choice of materials, geometries, and capacitances can all be varied to suit particular packaging requirements. The particular geometry of the embedded capacitors is very flexible in terms of their orientation, size, number, location, and composition of their constituent elements.

While embodiments have been shown in which signal traces are provided around the periphery, and in which Vcc and Vss traces are provided at the die core, the inventive subject matter ~~invention~~ is equally applicable to embodiments where the signal traces occur other than at the periphery, and to embodiments where Vcc and Vss traces are provided anywhere on the die.

Further, the inventive subject matter ~~present invention~~ is not to be construed as limited to use in C4 packages, and it can be used with any other type of IC package where the herein-described features of the inventive subject matter ~~present invention~~ provide an advantage.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that ~~which~~ is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the inventive subject matter ~~present invention~~. Therefore, it is manifestly intended that embodiments of this invention be limited only by the claims and the equivalents thereof.